IN THE CLAIMS:

1. (Currently Amended) A computer processor, the processor comprising:

(a) a decode unit for decoding a stream of instruction packets from a memory, each instruction packet comprising a plurality of instructions;

(b) a first processing channel comprising a plurality of functional units and operable to perform control processing operations responsive to control instructions dedicated to program flow and branch and address generation;

(c) a second processing channel comprising a plurality of functional units and operable to perform data processing operations;

wherein the decode unit is operable to receive instruction packets sequentially and to detect if each instruction packet is of a first class which defines (i) at least two said control instructions or a second class which defines (ii) a plurality of instructions one or more of which is a data processing instruction, the decode unit using at least one identification bit at a predetermined bit location in the packet for detecting if the instruction packet is of the first or second class, and wherein when the decode unit detects that the instruction packet comprises at least two said control instructions, said control instructions are supplied to the first processing channel for execution in program order, and when the decode unit detects that the instruction packet is of the second class, said plurality of instructions are executed simultaneously, and wherein said control instructions have a bit length less than said data processing instructions.

2. (Previously Presented) A computer processor according to claim 1, wherein when the decode unit detects that the instruction packet comprises three control instructions, the decode unit is operable to supply each of the three control instructions for execution in the order

in which they appear in the instruction packet.

3. (Previously Presented) A computer processor according to claim 1, wherein the decode unit is operable to detect that the instruction packet contains a plurality of control instructions of equal length.

4. (Previously Presented) A computer processor according to claim 3, wherein the decode unit is operable to detect that one of the control instructions in the instruction packet is of a bit length between 18 and 24 bits.

5. (Previously Presented) A computer processor according to claim 4, wherein the decode unit is operable to detect said at least two control instructions each having a bit length of 21 bits.

6. (Original) A computer processor according to claim 1, wherein the decode unit is operable to receive and decode instruction packets of a bit length of 64 bits.

7. (Previously Presented) A computer processor according to claim 1, wherein the decode unit is operable to detect when there is at least one data processing instruction in the instruction packet and, in response thereto, to cause relevant data to be supplied to the second processing channel.

8. (Previously Presented) A computer processor according to claim 1, wherein the decode unit is operable to detect that the instruction packet of the second class comprises at least one data processing instruction and a further instruction selected from one or more of: a memory access instruction; a control instruction; and a further data processing instruction.

9. (Original) A computer processor according to claim 8 wherein, at least one data processing instruction and said further instruction are executed simultaneously.

10. (Original) A computer processor according to claim 1, wherein the second processing channel is dedicated to the performance of data processing operations and data processing instructions are provided in assembly language.

11. (Original) A computer processor according to claim 1, wherein the control processing operations are performed on operands up to a first predetermined bit width and the data processing operations are performed on data up to a second pre-determined bit width, the second pre-determined bit width being larger than the first pre-determined bit width.

12. (Original) A computer processor according to claim 1, wherein the first processing channel comprises units selected from one or more of: a control register file; a control execution unit; a branch execution unit and a load/store unit.

13. (Original) A computer processor according to claim 1, wherein the second processing channel comprises a data execution path including a configurable data execution unit.

14. (Original) A computer processor according to claim 1, wherein the second processing channel comprises a data execution path including a fixed data execution unit.

15. (Original) A computer processor according to claim 13, wherein, in use, the configurable data execution unit operates according to single instruction multiple data principles.

16. (Original) A computer processor according to claim 14, wherein, in use, the fixed data

execution unit operates according to single instruction multiple data principles.

17. (Previously Presented) A computer processor according to claim 1, wherein the second processing channel comprises one or more of a data register file and a load/store unit.

18. (Previously Presented) A computer processor according to claim 1, wherein a single load/store unit is accessed by both the first processing channel and the second processing channel through respective ports.

19. (Previously Presented) A computer processor according to claim 1, wherein the decode unit is operable to detect that the instruction packet of the second class comprises at least one data processing instruction having a bit length between 30 and 38 bits.

20. (Previously Presented) A computer processor according to claim 19, wherein the decode unit is operable to detect that the instruction packet of the second class comprises at least one data processing instruction having a bit length of 34 bits.

21. (Previously Presented) A computer processor according to claim 1, wherein the decode unit is operable to detect that the instruction packet of the second class comprises at least one data processing instruction and a memory access instruction.

22. (Original) A computer processor according to claim 21, wherein the bit length of said memory access instruction is 28 bits.

23. (Previously Presented) A computer processor according to claim 1, wherein the decode unit is operable to detect that the instruction packet of the second class comprises at least one

data processing instruction and at least one control instruction.

24. (Previously Presented) A computer processor according to claim 1, wherein the decode unit is operable to detect that the control instructions are in C code or variant thereof.

25. (Previously Presented) A computer processor according to claim 1, wherein the decode unit is operable to detect that the data processing instruction is in assembly language.

26. (Currently Amended) A method of operating a computer processor which comprises first and second processing channels, each having a plurality of functional units, wherein the first processing channel is capable of performing control processing operations responsive to control instructions dedicated to program flow and branch and address generation and the second processing channel is capable of performing data processing operations, the method comprising:

(a) receiving a sequence of instruction packets from a memory, each of said instruction packets comprising a plurality of instructions defining operations;

(b) decoding each instruction packet in turn at a decode unit by determining if the instruction packet is of a first class which defines (i) at least two said control instructions; or is of a second class which defines (ii) at least one data processing instruction, and the decode unit using at least one identification bit at a predetermined bit location in the packet for detecting if the instruction packet is of the first or second class; and

wherein when the decode unit detects that the instruction packet comprises at least two said control instructions, supplying said at least two control instructions to said first processing channel for execution in sequence, and when the decode unit detects that the instruction packet is of the

second class, said plurality of the instructions are executed simultaneously, and wherein said control instructions have a bit length less than said data processing instructions.

27. (Previously Presented) A computer program product comprising a computer readable medium bearing a program code, which when processed by a computer, causes the computer to be operated according to the method of claim 26.

28. (Previously Presented) A computer readable medium bearing a program code, comprising a sequence of instructions for causing a computer to be operated according to the method of claim 26.

29. (Currently Amended) A computer readable medium bearing an instruction set for a computer including a first class of instruction packets each comprising two or more control instructions for execution sequentially, wherein said control instructions are dedicated to program flow and branch and address generation, and a second class of instruction packets each comprising at least a data processing instruction and a further instruction for execution contemporaneously, wherein instruction packets contain at least one identification bit at a predetermined bit location in the packet for detecting if the instruction packet is of the first or second class, and wherein said control instructions have a bit length less than said data processing instructions.